T7-1110/301
Deal No. AN67-3094
Copy 18

T7-1110/301

ONE-GIGABIT MASS MEMORY FOR ADA

VOLUME I
TECHNICAL AND MANAGEMENT PROPOSAL

North American Aviation, Inc. Autonetics Division

T7-1110/301
Deal No. AN67-3094

18

ONE-GIGABIT MASS MEMORY FOR ADA

VOLUME I
TECHNICAL AND MANAGEMENT PROPOSAL

18 May 1967

Approved By:

G.B. Way
Chief Engineer
Data Systems Division

North American Aviation, Inc. Autonetics Division

3370 Miraloma Avenue, Anaheim, California 92803

This data, furnished in connection with Request for Proposals No._____ _____ , shall not be disclosed outside the Government and shall not be duplicated, used, or disclosed in whole or in part for any purpose other than to evaluate the proposal; provided, that if a contract is awarded to this offeror as a result of or in connection with the submission of this data, the Government shall have the right to duplicate, use, or disclose the data to the extent provided in the contract. This restriction does not limit the Government's right to use the information contained in the data if it is obtained from another source without restriction. The data subject to this restriction is contained in Sheets 9, 10, 11, 12, and 13.

CONTENTS

ILLUSTRATIONS

FOREWORD

Autonetics is currently under contract to the Navy to design, fabricate, and deliver a Development Model of the MEM-BRAIN File. This file has been developed by Autonetics with major emphasis on the known requirements for mass storage devices applicable to military data systems. The present contract is for a model having a capacity of approximately two gigabits in a space substantially enclosable within a rectangular parallelepiped 24 x 24 x 41 inches.

We herewith propose a closely coordinated program to supply a similar model with one gigabit capacity and correspondingly smaller size, weight, etc., for application to the ADA program per RFQ from RCA/DEP dated April 28, 1967.

I. INTRODUCTION

A. PURPOSE

This document describes the current status of the Autonetics mass storage (MEM-BRAIN) program and additional efforts proposed to provide a MEM-BRAIN model suitable for use in the ADA system.

B. PRESENT PROGRAM

Autonetics is currently under contract to the Navy for the design, fabrication, and delivery of a developmental model MEM-BRAIN File under DCA sponsorship. The model to be delivered will have the final required form factor and will use parts approaching as nearly as possible those which would be used in the final production model. Also, the requirements covered by various military specifications will be met. This model will have the maximum capacity contemplated by Autonetics in the MEM-BRAIN File program, approximately 2×10^9 bits (two gigabits). The program involves a planned series of environmental tests of subassemblies during the period from mid-May through October of 1967. Subsequently, pre-qualification tests of the completed unit are expected to be performed.

The program involves engineering design, fabrication, and engineering test of the full scale unit based on the extensive development already carried out by Autonetics. During this development, the major design objectives associated with the MEM-BRAIN File concept have been identified. Problem areas have been subjected to analytical and experimental investigation sufficient to lead to the conclusion that the design objectives are feasible. Two fundamental principles have served as major guides in this development. The first of these is the choice of a simple solution in preference to a complex solution of any given problem including optimization of trade-offs on this basis. This principle has been emphasized because of the target objective of maximum reliability for the complete system. The second major principle has been the use of a close approximation to true kinematic design wherever it would serve to minimize the influence of external conditions on internal deflections, distortions, etc., which could influence the operation or reliability of the file.

Laboratory test and demonstration models of reduced capacity have been operated at Autonetics, including operation under computer control for a limited range of functions (see Figure 1). A number of qualitative and quantitative tests have been made during this phase of the program which improve confidence that the completed unit will be capable of withstanding military environmental conditions. For example, during early tests of the reproduction of simple bit patterns on a single track with oscilloscope display, the central member of the laboratory model which supports the moving head transport has been hit with a heavy soft-faced hammer to simulate a shock condition. Such shocks showed no visible evidence of affecting the data reproduction.

All the basic mechanical elements and principles of the two-gigabit MEM-BRAIN File remain unchanged for adaptation to units of smaller capacity. The major differences involve the number of disks with the resultant changes in overall length and possible re-engineering of spin bearing configuration for the shortest units. Of course, these changes also result in changes in overall weight and power requirements

of the different units. Furthermore, major differences in requirements for input/output capability can result in engineering modifications in the electronics package. Such modifications will in general be in the nature of simplifications which would lead to a reduction in cost of production; but the greater the change, the greater the additional engineering effort required to complete the modification. It should be noted, however, that the fundamental design has made provision for detailed adaptation to various computers with a minimum of change in the electronics, provided the fundamental requirements remain unchanged.

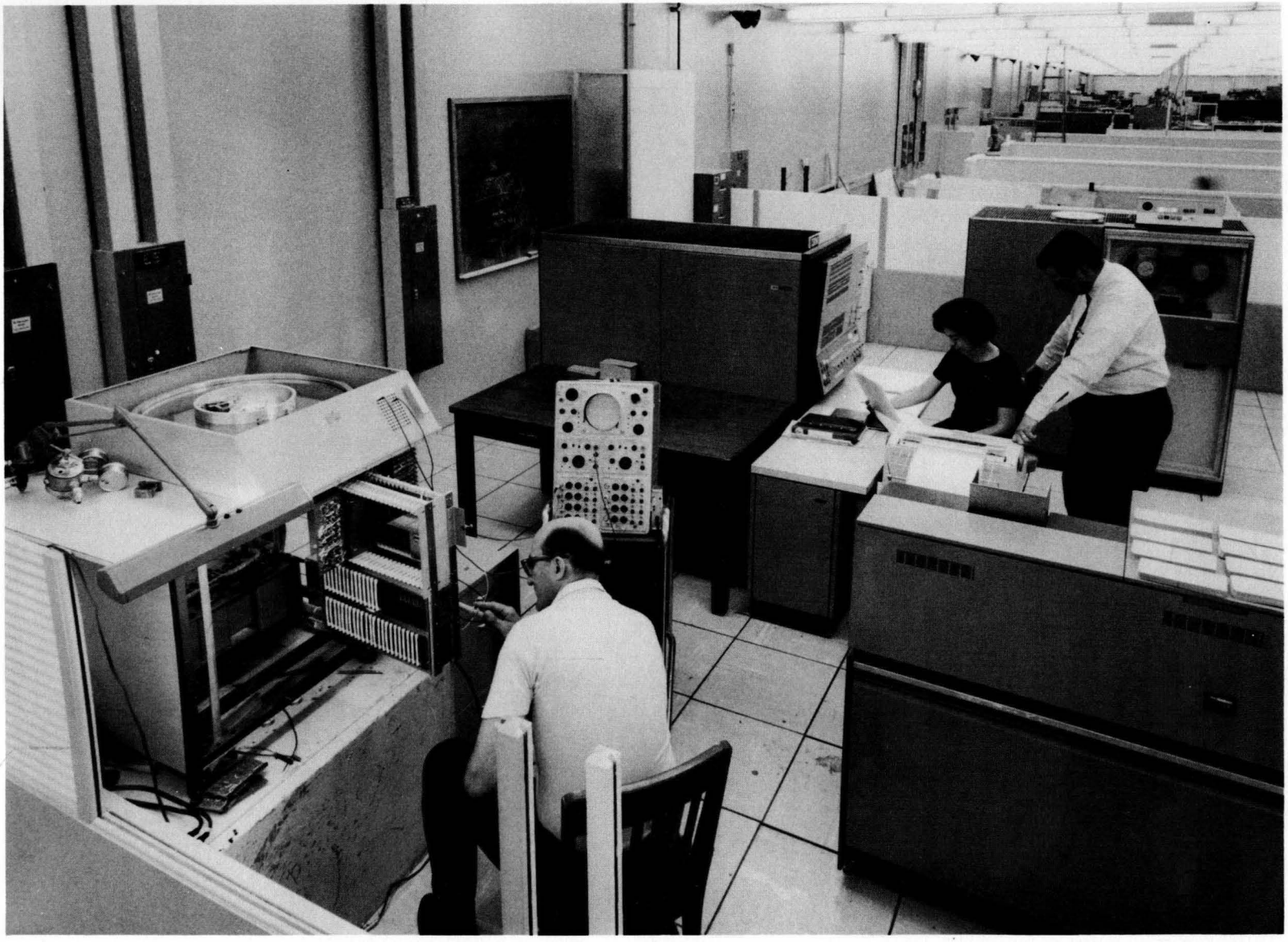

Figure 1. Computer Integration With Demonstration Model File

II. BASIC PRINCIPLES OF A MEM-BRAIN FILE

The MEM-BRAIN File is basically a rotating magnetic disk unit; but, beyond this point, it is different from all previous disk storage devices. The fundamental objective was to develop a mass storage unit with high reliability in a military environment. Therefore, maximum emphasis has been placed on high stiffness-to-mass ratios and low Q's in the mechanical structure, with overall functional simplification of the combined computer-file system. These principles have resulted in the adoption of an inside-out configuration making maximum use of prestressed elements to improve dynamic response and reduce weight and bulk of the unit. As a result, the disk surfaces are formed of thin stretched foil diaphragms whose form led to the adoption of the name "MEM-BRAIN" for the file. The resulting disk stack occupies little more axial length than is required for the support and control of the recording and reproducing heads between the disks, in contrast with conventional files where disk thickness need for rigidity adds a major fraction to overall length of a disk stack. In the electromechanical portion of such a system, parameter degradation and drift phenomena are negligible as sources of failure. On the contrary, mechanical damage or wear resulting from such environment factors as dirt, humidity, etc., if uncontrolled, are major factors in failure. Therefore, the MEM-BRAIN File has been designed with an essentially hermetically sealed enclosure for the electromechanical portion of the system. The objective of this seal is to maintain a substantially dry gas environment within the electromechanical package over a long period of military service.

Because electronic elements are more subject to catastrophic failure or performance degradation by parameter drift, these elements are located in a separate portion of the integral package which is dust- and drip-proof but accessible for maintenance by module removal and replacement. System optimization studies have shown that greater throughput could be accomplished if certain file processing features were included in the file to relieve the central computer from such detailed management. Since the configuration of the disk stack left an external disk surface available, it was decided to provide fixed head equipment accessing one end surface to provide short loop temporary storage, clock, and other similar functions. The extent to which this capability is provided remains subject to engineering modification for specific programs. The specific provision for external connection is likewise subject to engineering modification for a particular program. However, the basic plan involves the use of 64 duplex input/output (I/O) channels and changes would normally be made in increments of eight channels. Adaptation to the needs of different computers, on the other hand, will normally require only replacement of one or two circuit card modules.

III. SPECIFIC REQUIREMENTS FOR THE PROPOSED FILE

The proposed one-gigabit unit differs from the two-gigabit file of the Navy contract in the following particulars:

1. There will be only 31 disks in the stack rather than the 61 planned for the current contract.

2. The overall length of the unit will be approximately 27 inches rather than 41 inches.

3. Design goal will be 250 pounds rather than 400 pounds.

4. Estimated power requirements will be 1700 watts rather than 2700 watts.

5. The unit will have the same I/O and internal processing capabilities as planned for the Navy file.

Because of the minimum nature of the electronic design changes, modification engineering for this unit will be relatively small. The change in length will not affect the fundamental spin bearing requirements sufficiently to require major engineering effort; and the reduction in number of arms requires only minimal changes in the switching and control logic.

IV. FILE DESCRIPTION

A. FILE INTERFACE

The internal organization of the file is illustrated in Figure 2. Four control resistors, each associated with its block of 16 I/O data channels, simultaneously control the switching of the heads. They also accept and transmit the instructions in control of internal data manipulation. Discrete control lines commit instructions and data, and deliver file status as required. The external function request is therefore available if the I/O channel or I/O control register is not otherwise busy and an instruction may be transmitted. Depending upon the execution time of the particular command designated in the instruction, the file and central processor unit (CPU) will alternately and asynchronously signal to each other their readiness and acceptance at each data sampling period. There are four output discretes and five input discretes. Also operating on the controller is a Security Code, which is part of the instruction word, and when in effect, requires a match to allow the function to proceed.

Four I/O buffers each present eight binary inputs and eight binary outputs through a multiplexer to the parallel word I/O register. Two I/O channels contain 37 parallel duplex data lines and two contain nine such lines including parity. These data lines are capable of asynchronous transfer of instructions and data. The transfer rates are limited only by the size of the static buffer (256 8-bit bytes in two folded buffers per I/O channel), the 338-KC clock rate, and the file processing time where processing is involved. Alternatively the file is also capable of transfer of 6 bits plus parity via 7 duplex data lines.

Special conditions related to busy condition of head arms, priorities by other connected CPU's, etc., are determined internally and expressed indirectly through the four output control lines. Other file intelligence such as transfer error conditions is available even if not usable by the connected CPU. Differences in the number and functions of discrete control lines of different CPU's require only the replacement of certain plug-in modules to bring interface conformance of the file. Beyond this, the file's internally stored program is under program control of the connected device. Where the input/output levels and impedances are not compatible, a plug-in module change is again necessitated.

B. SOFTWARE

Operation of the file is directed by an instruction fed over the input data lines into an I/O control register. This binary numbered instruction contains segments designating arm, head, track, and sector number, I/O channel address, and the command codes. The multiplexing introduced to implement selection of the I/O channel also makes the Static Buffers available as additional temporary storage for internal data manipulation. Under such circumstances, communication between the file and the CPU may be temporarily interrupted, but without serious consequence because of the internal stored program and independent bookkeeping capability of the file.

Each instruction contains the command code and tags such as block address, length of record, I/O channel address, terminal code, match criterion, descriptor, operand address, etc., which are the command modes. The command code establishes the sequence of modes limited by the tags.

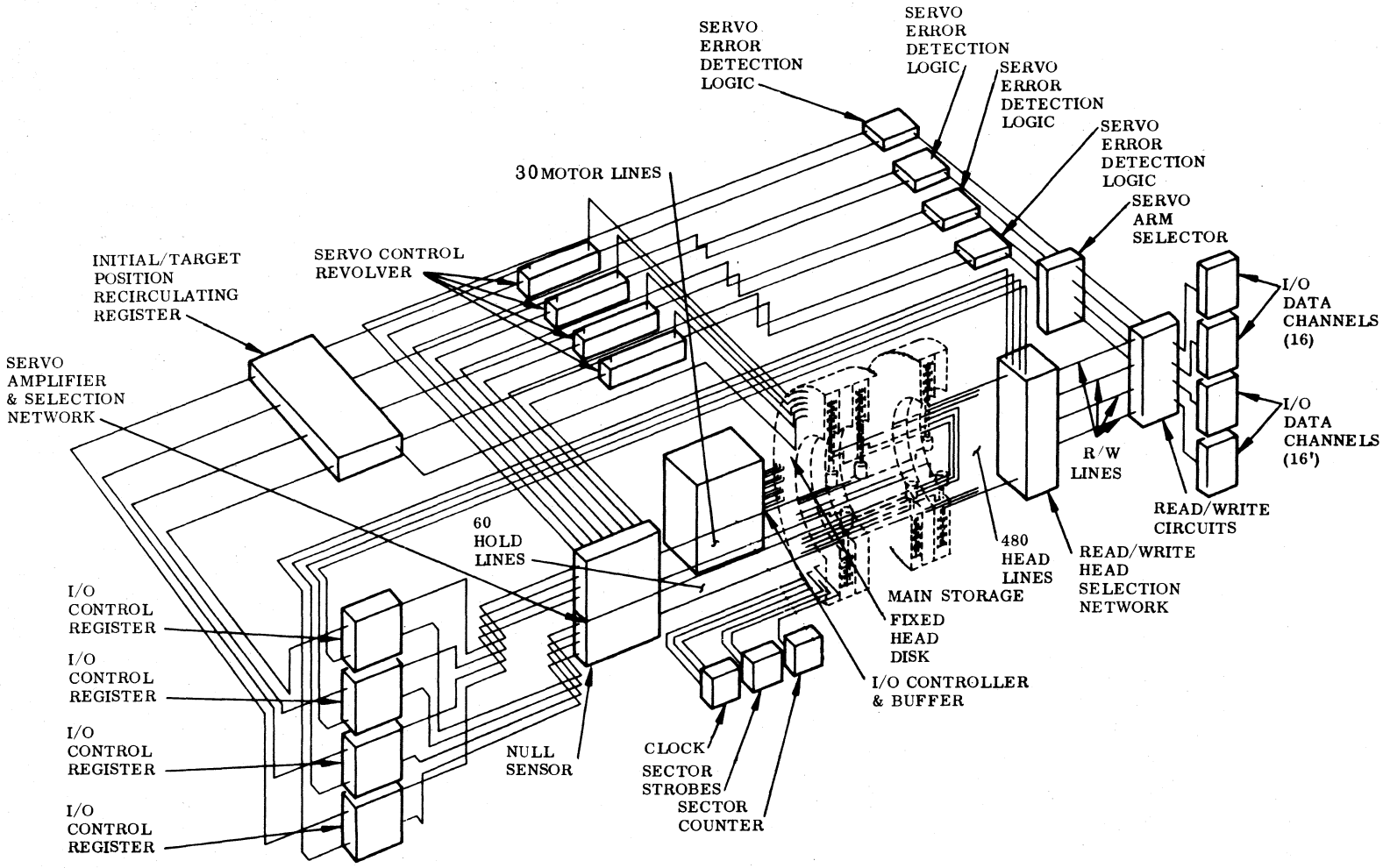

Figure 2. Functional Schematic of 30-Arm Digital Disk File

The beginning and end of blocks of data are addressed according to sector. Addresses are also affixed for each sector. The number of sectors, or length, is predetermined to correlate to the fixed head recirculating registers. However, the sector count can be changed, but only in a modular relationship to the fixed head loops. Thus, the word length, if carefully planned, will avoid waste of space between sectors, or data blocks. But, in any case, the CPU is not bound to transmit or receive full sector length of data. It is also notable that the memory is addressable to a byte.

The reading or writing on heads associated with any arm may occur while servoing any other arm. With minimal interference, data may also be accessed by more than one CPU (or inquiry station), or may simultaneously output to peripheral equipment. The file may be operated so that all storage is available to all externally connected devices, or it may be operated with different organization in different parts of the machine so that it looks like several independent auxiliary stores to the externally connected systems.

C. ELECTRONICS AND LOGIC

The basic storage function is accomplished on the disks accessed by movable heads. The built-in control functions are implemented by the fixed head elements and associated electronics. The clock and origin is unalterably recorded on fixed head tracks.

The fixed head elements with electronics are used for implementing the control and processing functions with occasional possible use of the Static Buffers. Other electronics include read and write amplifiers along with the multiplexed switching networks. Also included is the servo electronics which is multiplexed between the 60 head positioning arms and the four I/O control registers on an "as available" basis.

The servo amplifiers respond to a difference signal developed by detecting the phase of different tracks recorded 90 degrees relative to one another. Coarse positioning of the arm servo is controlled by determining the tracks traversed. Fine positioning is controlled by adjacent track nulling. Track identification, which is recorded in each sector, verifies location (eight bits).

The electronics includes counters, compare logic, etc., to a point short of performing arithmetic operations. Internally, the electronics acts completely in synchronism with the clock. NRZ recording is used throughout. These characteristics allow simultaneous transfer of all data lines (internal and external) in synchronism with one clock. Internal control and processing takes place, however, serially by byte, or bit, as may be required.

All circuitry consists of replaceable microminiaturized circuit board assemblies to withstand military environments with excellent MTBF and MTTR. Each assembly contains less than 50 integrated circuits.

D. MECHANICAL

Mechanical design of the file centers about the high stiffness-to-mass ratio of a pre-tensioned diaphragm, both for the disks and for the principal support structure of the rotating mass (the disk stack). This principle leads to an inside-out form for

the disk. The disks are mounted and rotated from the periphery and accessed from the center, as shown in Figure 3. The disks are thin annular sheets of magnetically plated foil, each stretched taut over a tensioning hoop. The tensile preload established by this process causes the magnetic plated diaphragm to act as a rigid surface of uniform flatness; this eliminates surface finishing operations. Such a diaphragm tolerates extreme thermal variations without distorting out-of-plane. The disk has a mass two orders of magnitude less than a conventional disk. These properties of the disk are basic to the militarized qualities of the file.

The disk stack forms a cylinder which is closed around the periphery, thus concentrating the major mass at the periphery. This disk stack is directly driven by a synchronous motor which combines with the high moment of inertia-to-mass ratio of the disk stack to provide a highly uniform rate of rotation. One end of the disk stack is constructed of a pre-tensioned pair of shallow-coned metal sheets. This forms a light end bell providing extremely high rigidity in both the axial and radial planes. The end bell is carried by a bearing supported by a similar conical pair. Three degrees of freedom are thus constrained. The other end of the disk stack is supported by a bearing through a membrane structure providing a two degree of freedom constraint. Thus, the total mechanical system provides a mechanism having high natural frequency and low vibration amplitude. By judicious application of visco-elastic coatings, the mechanical Q of the total structure is kept below one.

Each movable head arm consists of a light tubular member supported on an internal gas bearing and driven by a servomotor. Each tubular member carries eight read-write heads with suitable means for forcing them toward the facing surfaces of two disks (four heads per disk surface). The heads are attached to pads which furnish an air bearing support to maintain accurate spacing from the rotating disk surfaces. The entire assembly is supported by a rigid structural member attached to the central frame of the disk unit. The four heads facing one disk surface are equally spaced at a separation corresponding to the zone width of the record pattern. Therefore, the distance through which the servomotor must drive the heads is one zone width (256 tracks).

Each arm is equipped with a clamp which holds the arm in position once the servo has attained the proper location. By this means, the electronic elements of the servo can be released and switched under I/O register control to position other arms.

A group of fixed heads is located at one end of the disk stack. These head-pad assemblies are also air bearing supported at the surface of the disk. The head assemblies are supported by rigid structural members attached to the central structure and are spaced to provide rapid access recirculating loop capability. Functionally, the support for these fixed heads is equivalent to a solid headplate, but it is structurally segmented to permit removal and replacement without disturbing the disk stack.

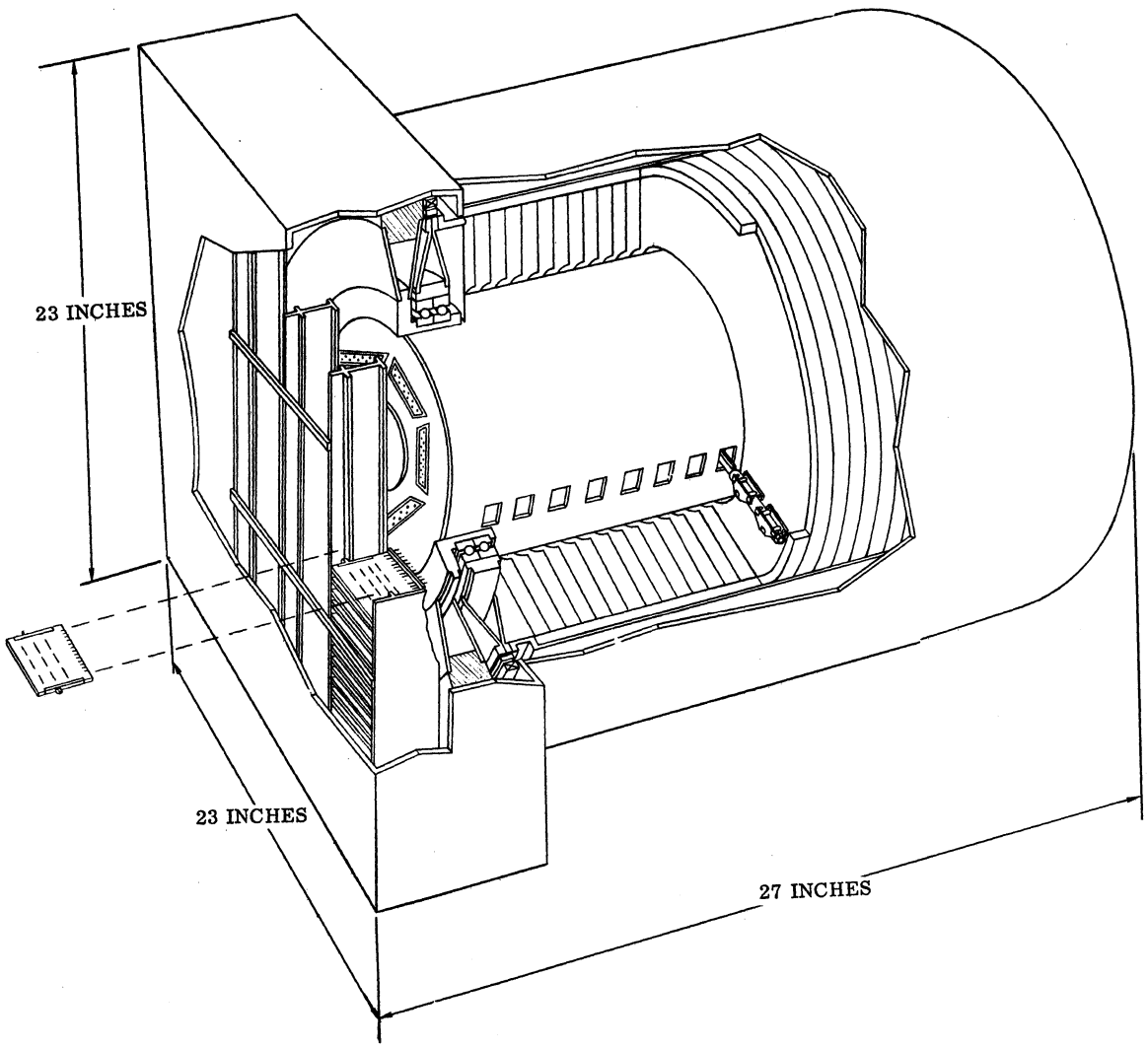

Figure 3. One-Gigabit Digital Disk File

V. RELIABILITY

A. DESIGN FOR RELIABILITY

The design principles embodied in the file were selected with the ultimate reliability of the device in a military environment as a paramount consideration. Simplicity is always of extreme value in eliminating failure modes and enhancing reliability of any system. Consequently, at every point where a choice between simple and complex solutions was available, the simpler technique was chosen.

The electromechanical elements of such a device are known to be sensitive to adverse environments related to humidity, pressure, and temperature. The electromechanical package was designed as a hermetically sealed unit, and care was taken in the choice of materials and their structural interconnection to minimize disturbance of critical locations due to temperature or temperature gradient.

The electronic elements of such a system, on the other hand, may be more subject to deterioration in performance by parameter drift or catastrophic failure. Therefore, the electronic package was designed for ready access to permit maintenance by module replacement. Its enclosure will be dust-proof and drip-proof, but will not be hermetically sealed.

To minimize the failure potential in the electronic system, the background developed on the Minuteman standard parts will be used whereever applicable with judicious regard to schedule and cost.

B. PREVENTIVE MAINTENANCE

In addition to the care taken in selecting the design features specifically to improve the inherent reliability of the file, a preventive maintenance program will be established to enhance reliability. Such a program will be based on a philosophy of substitution maintenance where the serviceman has available a stock of spare modules and a checklist giving an optimum routine for such procedure. It is expected that the preventive maintenance program will call for this operation at scheduled intervals (about once every 1000 hours). If a failure were to occur, the preventive maintenance routine would follow upon correction of the failure, thereby extending the next preventive maintenance to 1000 hours thereafter. The hermetically sealed electromechanical package will not require maintenance except at extremely long intervals. Such maintenance should not normally be attempted except under clean-room conditions.

C. TEST PROGRAMMING

The results of the environmental test conducted on subassemblies in accordance with the milestone chart, Figure 4, will be used to verify the design from the reliability point of view as well as the functional point of view. These tests are being conducted informally at Autonetics for the purpose of insuring subsystem design integrity; these tests (Category I) will not be a bid item in this proposal.

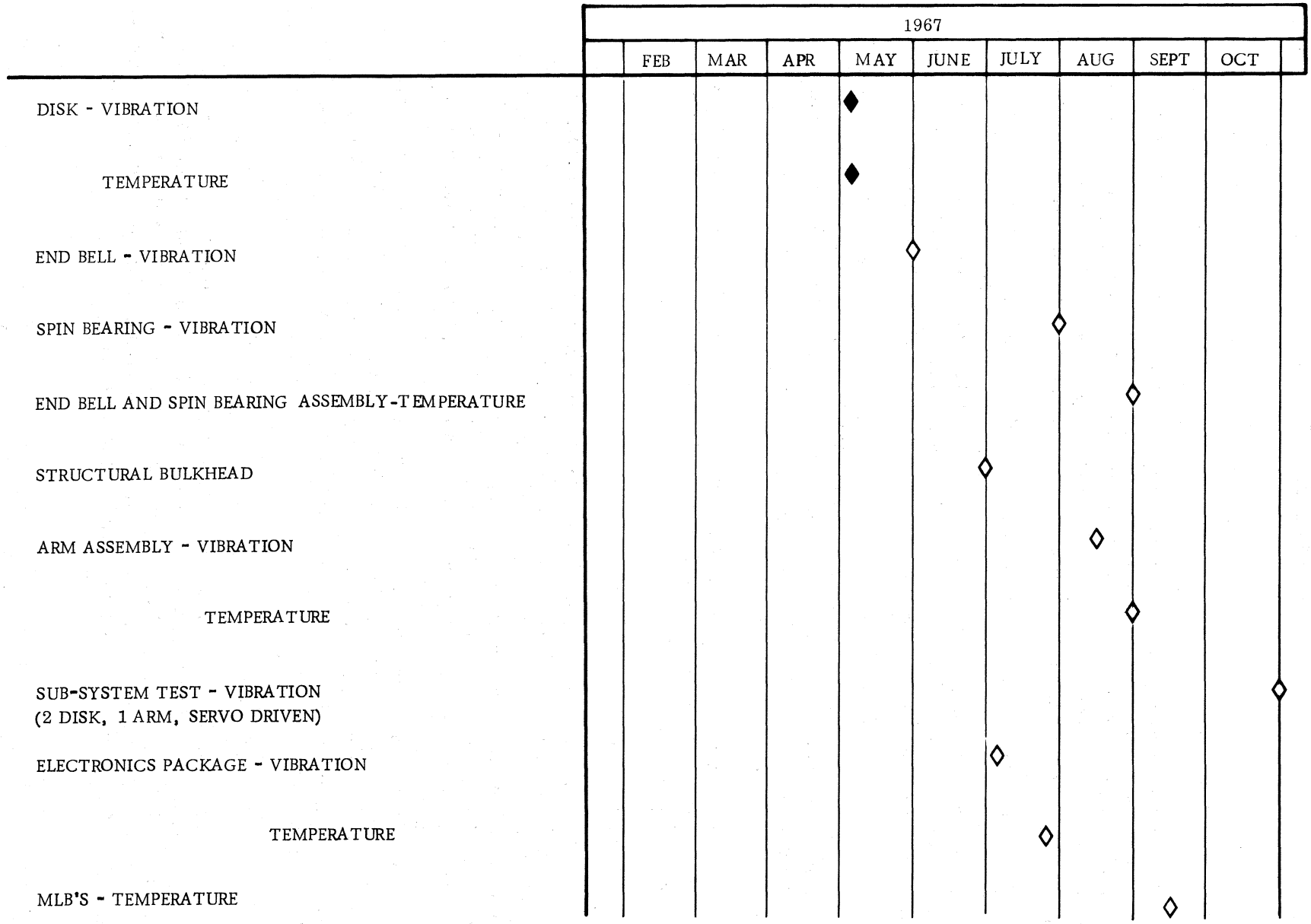

Figure 4. Milestones: Environmental Tests, Subassemblies

VI. ORGANIZATION AND MANAGEMENT

A. INTRODUCTION

The following sections present Autonetics', management approach to assure full accomplishment of all objectives set forth in the cost proposal.

The file design and fabrication will be accomplished within the Data Systems Division, a product division of Autonetics. As outlined in Figure 5, North American Aviation, Inc. is composed of a number of operating divisions, including Autonetics. Operating division presidents are corporate vice presidents. The Autonetics operating division is in turn composed of product and management divisions, whose general managers are vice presidents of Autonetics. This structure makes the resources of the entire corporation available as needed in support of a program undertaken by any division. Each product division has its own manufacturing, engineering, quality control, logistics, material, marketing, contracts and pricing, and administrative organizations.

Autonetics, for many years, has been engaged in the research, development, design, test, and manufacture of lightweight, high reliability precision electronic and electromechanical equipment for a variety of military and space applications. The proposed design, fabrication, test, and evaluation efforts for the file are directly in line with this experience and the immediate interests of the corporation.

B. PROGRAM MANAGEMENT TEAM

The major emphasis during the design, fabrication, test and evaluation phases will be centered in the Engineering activities. An Engineering Program team has been established as shown in Figure 6. The team members have been named and resumes for each are included. Each was selected because of demonstrated success in performing work closely related to the objectives of the proposed program.

C. PROGRAM PLAN

Design and construction of the Exploratory Development Model of the One-Gigabit Digital Disk File will conform to those applicable portions of the Military Specifications, as set forth in the cost proposal, with pre-qualification tests performed by Autonetics personnel at the Autonetics facility.

Electromechanically the unit is as similar as possible to the present Autonetics MEM-BRAIN and the Naval Ship Systems Command (NSSC) Digital Disk File. The program is coordinated with the contract from NSSC for the Two-Gigabit Digital Disk File, and must proceed simultaneous to, or lag, the said NSSC contract. Mechanical and electronic subassembly designs of the NSSC contract will be used virtually as-is in the One-Gigabit Disk File program. The unit contains all of the data manipulation system of the Two-Gigabit Digital Disk File.

An Operations and Maintenance Manual containing descriptive expository data on the file will be provided. Together with periodic progress reports, this will comprise most of the documentation delivered. The major milestone chart is shown in Figure 7.

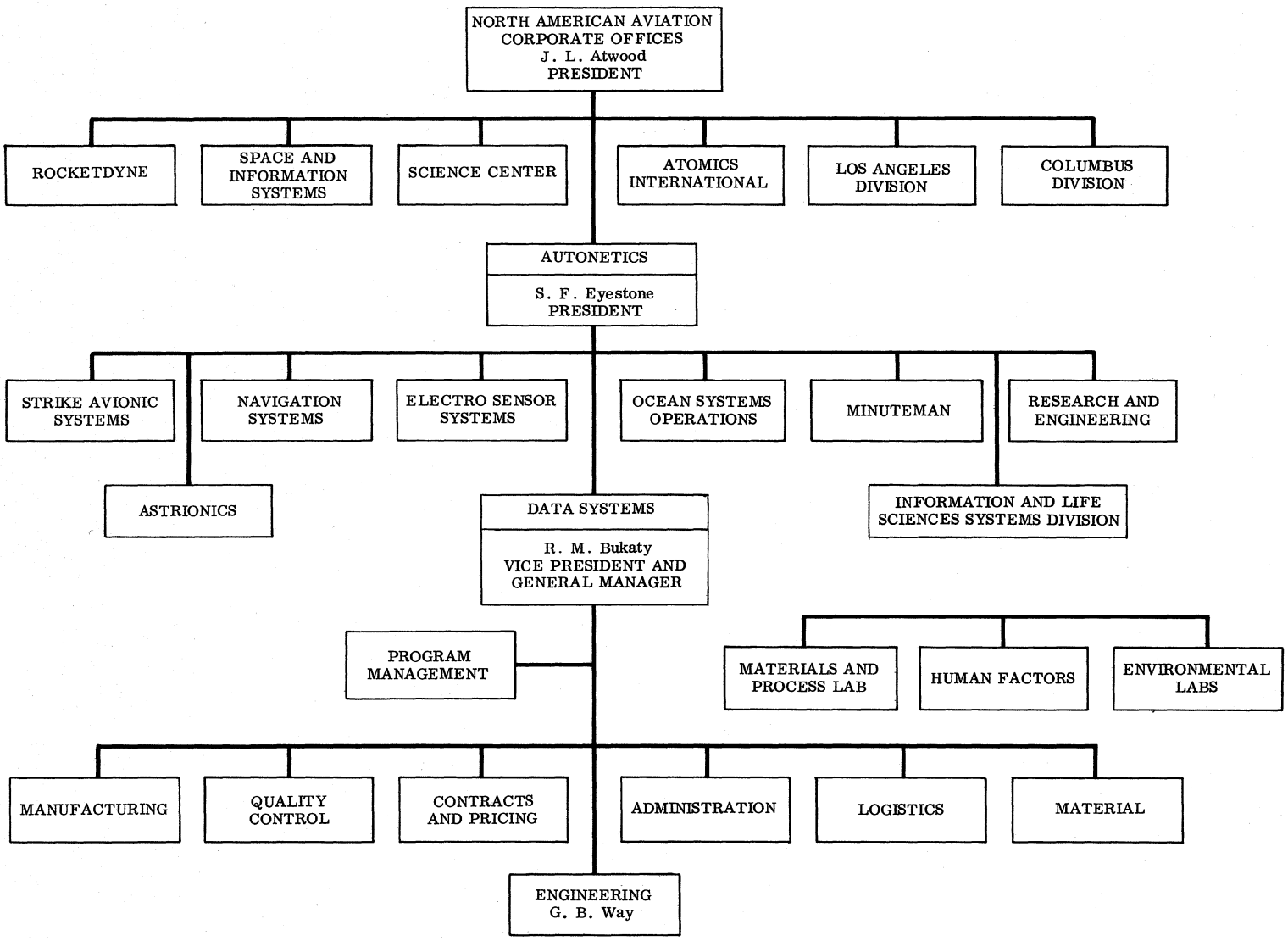

Figure 5. Corporate Structure

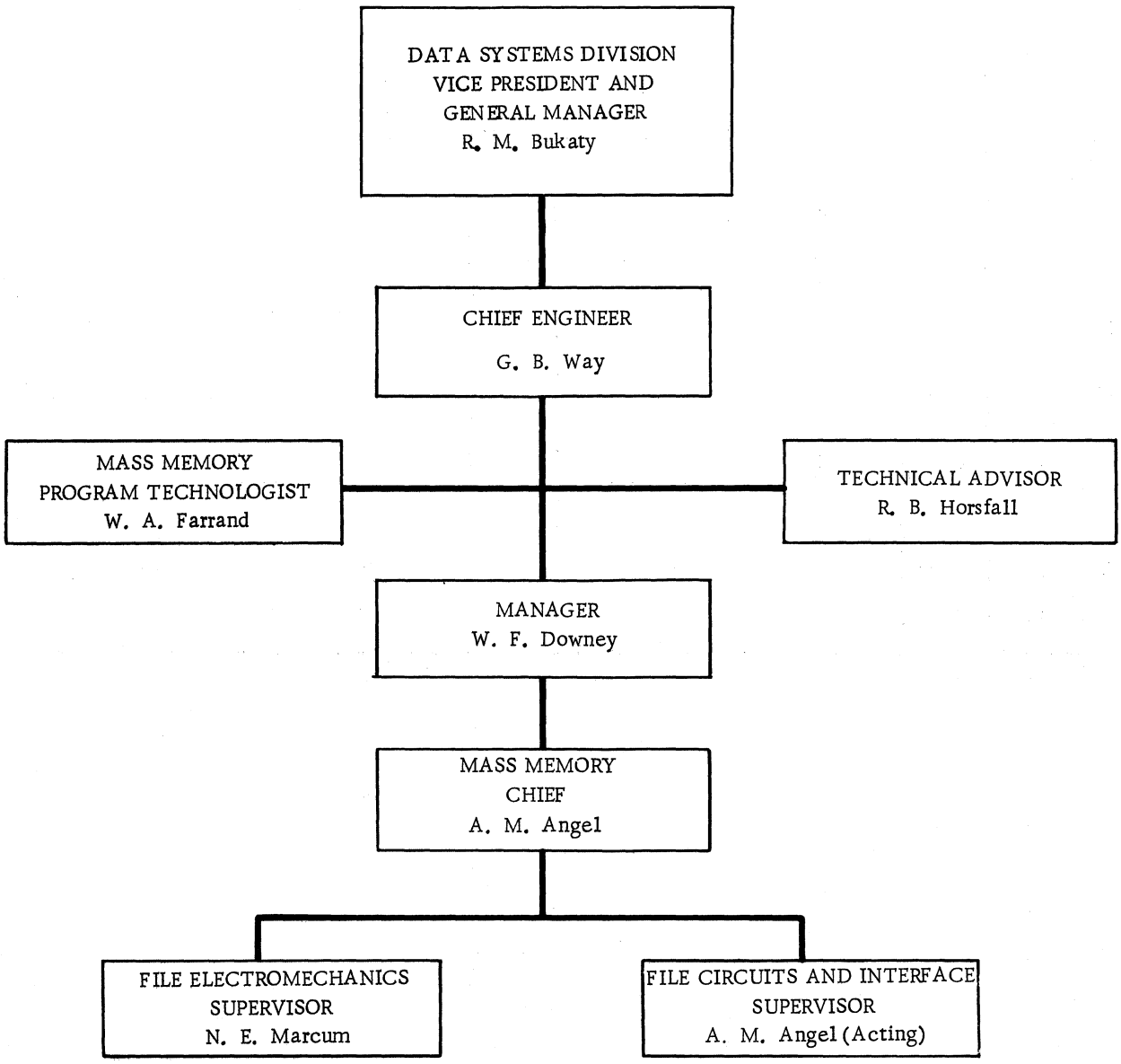

Figure 6. Digital Disk File Project Team

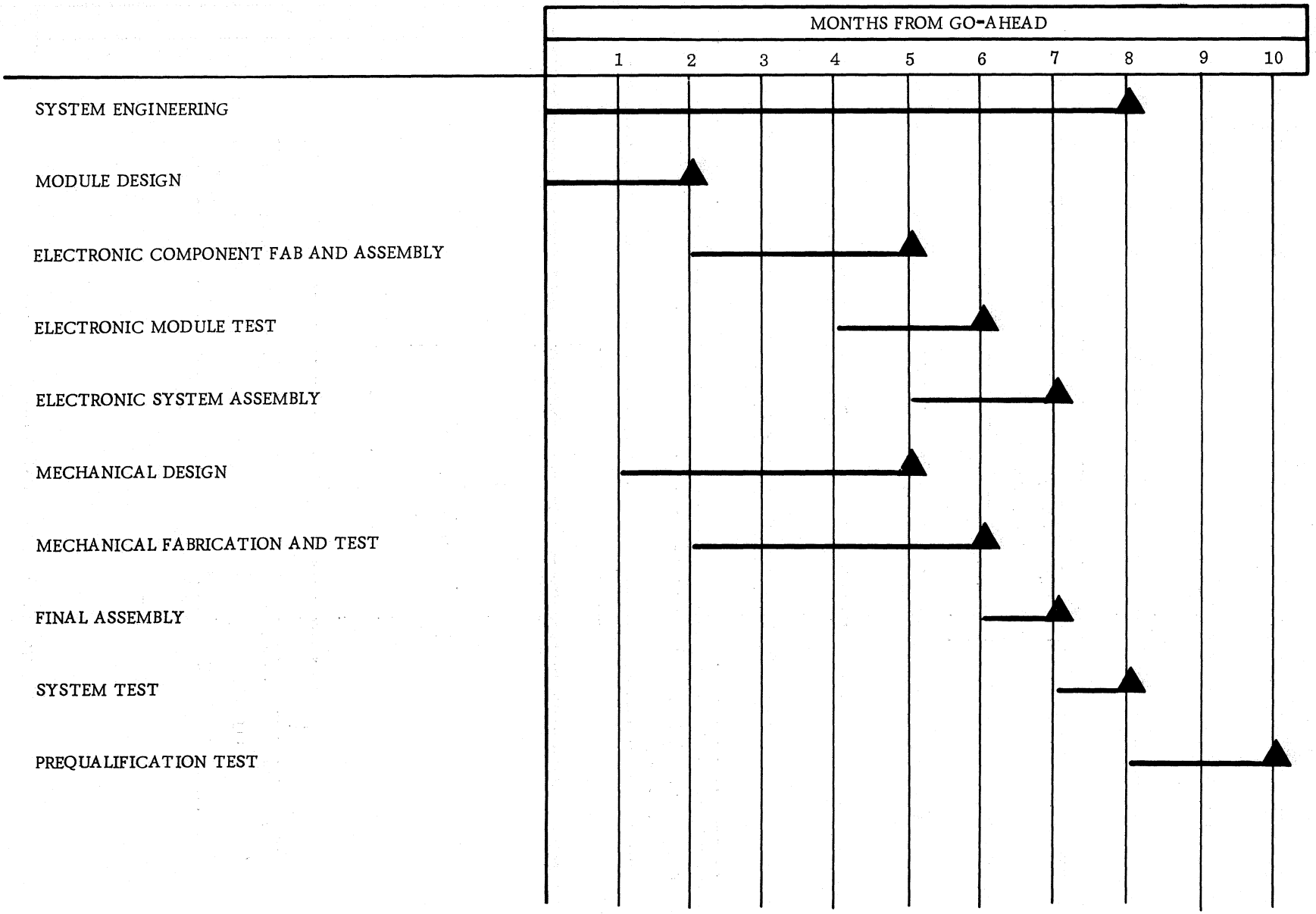

Figure 7. One-Gigabit Disk File, Major Milestones

D. EXPERIENCE AND BACKGROUND

1. Computers

In 1952, as part of the Navaho missile guidance system, we developed the NATDAN computer for use with an inertial platform. Our second major guidance computer was the VERDAN (Versatile Differential Analyzer). More than 1700 VERDAN's have been produced for use with the A-5C (A-3J), AGM-28 (GAM-77) Hound Dog Missile, and several classified airborne programs under ASD management. They are also used with Ship's Inertial Navigations Systems (SINS) on Polaris submarines and aircraft carriers. Production rate on the VERDAN reached a high of 50 per month.

Most recently, we developed the first production model microminiaturized computer -- the Autonetics D37 Minuteman II Computer. We also built the Automatic Ground Equipment for the Minuteman weapon system. These equipments are currently in production. D37 succeeds the Autonetics D17 (Minuteman I) Computer which we also designed, developed and produced. More than 1600 of these computers have been delivered. No primary failure has been assessed against the D17 during more than 65 firings of the Minuteman.

2. Disk Memories

Over 3500 production computers built by Autonetics, since 1948, have each included a disk memory. Autonetics' Data Systems Division is responsible for basic development of air bearings and heads for use in disk memories. We initiated the first special rugged disk memory designs for militarized computers.

We designed and built:

1. The first disk memory used in a military computer
2. The first disk memory used in a transistorized computer
3. The first disk memory computer used for submarine navigation
4. The first disk memory computer to guide a missile
5. The first disk memory designed to meet Minuteman-required MTBF (In actual performance, these units have surpassed the reliability requirements by more than a factor of three.)

E. CAPABILITIES

The projected workload of the Data Systems Division during the concerned time period will readily accommodate the added load of the proposed program. Necessary skills and experience will be available.

All necessary facilities to support the proposed effort are available and described.

1. MEM-BRAIN File Development Laboratory

The following equipments and facilities support the current development of the MEM-BRAIN Disk File and will be available for the Digital Disk File program.

a. Foil Preparation

1. Foil Storage and Handling Equipment
2. Foil Inspection Equipment
3. Foil Cutting
4. Foil-Hoop Thermal "Bonding"
5. Hoop Trimming
6. Packaging and Shipping Station

b. Disk Preparation

1. Receiving Inspection
2. Foil Pretrimming Equipment
3. Stretch Form Die Foil Holder
4. Stretch Form Die System
5. Concentricity-Flatness-Tension Inspection Equipment
6. I.D. Truing and Reference Diameter Forming Equipment
7. Magneform Foil Former

c. Servo Motor Dynamic Response Test

1. Power Supplied (2)
2. Oscillators (2)
3. Oscilloscope
4. Drive Motor Jigs and Fixtures
5. Dynamic Position Measuring System
6. Power Drive Controller

d. Disk Magnetic Characteristics

1. Hysteresograph
2. Head Tester

3. 12" Plated Foil Tester

4. Clock and Sector Writer

5. Signal Modulator and Demodulator Experimental Determination Setup

6. Precision Head Assembly Area

2. Disk Memory Assembly Shop

The disk memory assembly shop is a 7530 sq. ft. environmentally controlled area constructed at a NAA capital expenditure of $170,000. Equipment such as steri-shields, microscopes, ultrasonic cleaning devices, curing ovens, precision gauges, special work stations, etc., was provided at a NAA capital expenditure which exceeded $200,000. The dust is controlled within the area to below 500 particles per cu. ft. (under 5.0 microns). Over 3350 disk memories have been fabricated in this facility at a peak rate of 82 per month. A portion of the pre-production engineering prototype disk memory facilities will be used in the fabrication of the file.

3. Precision Assembly and Engineering Machine Shop

The precision assembly area, which is adjacent to the disk memory assembly shop, includes diamond laps, optical flat measuring devices, Swiss jig borer, micro-hone, stereo microscopes, air and electrical microinch measuring equipment, precision grinding facilities, Swiss rotary tables, and precision optical head alignment equipment.

The Engineering Machine Shop is fully equipped with mills, lathes, boring machines, etc., required to fabricate the detailed parts which comprise the disk file. This facility has been used in the engineering development of Autonetics computer disk memories.

4. Geographically Centralized Microelectronics Facility

The facility, constructued in 1963, provides the photographic and processing techniques for fabrication of multilayer boards (MLB's) and for joining integrated circuits to the MLB's. The area (22,000 sq. ft.) is both temperature- and dust-controlled. The dust is held below 500 particles per cu. ft. in the 5 to 65 micron range with no more than 10 particles exceeding 65 microns in size. This degree of control is essential for building microminiaturized equipment.

An $85,000 automatic X-Y plotter is available for the generation of accurate, aligned artwork used to produce MLB's. The plotter is capable of holding a location tolerance of ±0.001" across a 60" x 48" table.

Approximately 5500 sq. ft. of the facility contains the precision photographic equipment (e.g., a $22,000 Robertson Camera, a $13,000 Step and Repeat Camera, an $8000 Second Reduction Camera, and an $8000 Coordinatograph) to produce the reduced photo artwork.

5. Multilayer Board Fabrication

The development of the MLB's which provide the interconnecting network between the integrated circuits (IC's) has been accomplished in a 3200 sq ft portion

of the Microelectronics Facility. It contains the ultrasonic cleaning equipment, etching, photo resist, laminating, and plating facilities required to accomplish this effort.

The technology gained in this laboratory has been transferred to the 10,000 sq. ft. MLB production facility.

The Memory Production Facility occupies 2000 sq. ft. and is enclosed with ceiling-high walls. The temperature is controlled to 70^{o} ±5 F with the relative humidity controlled below 50 percent. The light intensity is held to a minimum of 125 ft-candles.

6. Environmental Test Facilities

The Environmental Test Laboratory, part of the Autonetics Research and Engineering Division, is housed in a 72,000 sq. ft. single-story building. This laboratory contains all of the facilities required to test the systems in the environments specified. These capabilities are:

Shock	Max 75 g's; 64-in. drop Duration 6.5 to 32 ms Max load 400 lb
Explosion	Simulates sea level to 80,000 ft. Combustible mixture of butane and air 4 ft. dia. x 5 ft. long chamber
HFI	Shielded enclosures 32 x 16 x 10 ft.; 56 x 12 x 8 ft.; 15 x 8 x 8 ft.
Temp. Altitude	-100 to +400 F; to 250,000 ft.
Vibration	Sine and Random Vibration systems 1500, 3000, 5000, 7500, and 30,000 force lb
Humidity	Temp 32 to 200^{o}F Rel humidity 20 to 100 percent
Salt Spray	Temp 95 F; salt solution 3-20 percent ph 6.5 to 7.2
Sand and Dust	Temp 77 to 160^{o}F; air velocity 200 to 2300 fpm; humidity less than 30 percent
Fungus	Temp 86 F; humidity 100 percent

F. PERSONNEL

Resumes for personnel on this program follow:

A.M. ANGEL, Chief, Mass Memory Section, Data Systems Division

joined Autonetics after two and one-half years as a consultant specializing in design and analysis of computer peripheral equipment. A few of his more important clients

were Minnesota Mining and Manufacturing Company, Bunker-Ramo Corporation and Raytheon Computer. Previously he was Director of Product Development, Tape Memories, for Ampex Computer Products Company. For 11 years he was with the National Cash Register Electronics Division as Chief Systems Engineer, Electromechanisms, responsible for the development of numerous devices such as random access memories, an optical character reader, a very high speed paper tape reader, a magnetic tape editor, a disk memory, drum memories, an electronic accounting machine, and a number of other less significant devices. He has been granted several electronic, mechanical, and systems patents and has presented papers, one of which is included in the book, entitled, "Large Capacity Memory Techniques for Computing Systems," published by The MacMillan Company. He served in the Air Force during World War II as an aircraft mechanic and electrical specialist.

Mr. Angel received a B.S. in engineering from UCLA. He is a member of the Professional Group on Electronic Computers of the IEEE. He has variously served on committees such as the ASA X3-1 Committee on Optical Character Recognition, the EIA TR-27.6.3 Subcommittee on Magnetic Tape, and the AIEE Computer Systems Subcommittee.

W.A. FARRAND, Assistant to the Chief Engineer, Data Systems Division (Co-inventor of MEM-BRAIN File), Program Technologist,

has been with Autonetics for 15 years. He is responsible for new computer and peripheral equipment business. Previously Mr. Farrand was Supervisor in charge of computers for the first inertial navigation systems (X-2, X-2A, 2-B, 2-C, X-4, X-5, and N-5A). As a Design Specialist, he developed the rotating magnetic disk memory. He was the initial Project Engineer on the Minuteman and VERDAN computers. He has performed extensive research, been granted numerous patents, and presented many technical papers on air bearings, analog-to-digital converters, displays, plotters, and printers. He wrote the chapter on input/output equipment for the McGraw-Hill Computer Handbook. He served in the Navy during World War II, working with electronics, radio, radar, and encrypting equipment.

Mr. Farrand received a B.A. degree in chemistry and an M.S. degree in electrical engineering from UCLA. He was an original member of the staff of the UCLA School of Engineering where he formulated and taught many undergraduate engineering courses. He is a member of the Association of Computing Machinery, AAS and Instrument Society of America, Chairman of the Digital-Differential Analyzer Council, and a member of the Board of Directors for Simulation Councils, Inc.

DR. R.B. HORSFALL, Senior Scientist, Command and Control Programs, Technical Advisor,

has, during his 18 years at Autonetics, been primarily concerned with advanced research and development programs as a Research Specialist, a Staff Engineer, a Group Leader, and a Senior Scientist. For two years. Dr. Horsfall served as a special coordinator for the Minuteman program. In 1961 he served for one year at the Pentagon on a special project with the Weapon System Evaluation Group. His prior experience includes one year each with the Army Ground Forces Board at Fort Knox, Kentucky as an optical physicist and as an optical engineer at Eastman Kodak; ten years at Bausch and Lomb; and, prior to graduate work, one year as a member of the technical staff at Bell Telephone Laboratory.

Dr. Horsfall received a B.S. degree from Reed College, and M.A. and Ph.D. degrees from the University of Illinois. He holds several patents in the fields of optics and automatic navigation, including a basic patent on stellar inertial navigation systems, and has written a number of scientific and technical papers. Dr. Horsfall is a member of the Optical Society of America and Sigma Xi. He was a contributing author to the McGraw-Hill book on Inertial Navigation edited by C. F. O'Donnell.

N.E. MARCUM, Supervisor, Electromechanics, (Co-inventor of MEM-BRAIN File),

is responsible for all Autonetics design and development work on rotating magnetic memories. He has been responsible for the design of these memories since 1954. During seven years with Remington Rand Univac, he developed memories and designed many protions of digital computers, peripheral equipment, and other complex electro-mechanical devices. His earlier experience consisted of eight years of design of automatic and semi-automatic machinery for several companies.

Mr. Marcum received his B.S. degree in mechanical engineering from the University of Minnesota in 1939. He holds, and has pending, many basic patents fundamental in disk memory technology.

T.M. HERTZ, Senior Technical Specialist, Logic and Programming,

has, during his 13 years at Autonetics, been engaged in operations relating to programming and logical design of digital computers. He had the sole resonsibility for the logical design of the RECOMP I, II, and III, as well as the JUKEBOX and REPAC computers. In addition, he has conducted investigations in the applicability of modular arithmetic and advanced logic techniques to Autonetics digital computers.

Mr. Hertz was a programmer for Remington-Rand, working with UNIVAC I. He taught physics at New York College of Engineering. As an instructor with the Air Force Technical Schools during World War II, he taught a variety of mathematics and electronics courses. He also worked as a technical writer.

Mr. Hertz received his B.S. degree from the College of the City of New York and his M.S. degree from New York University. He is a member of the Association for Computing Machinery and the Professional Group of Electronic Computers of the IEEE.

R.G. LARSON, Research Specialist, Data Systems Division,

is recently from Astrodata Inc., where for six years he served as project manager on large Data Acquisition Systems. During the course of these duties he was involved in the detail circuit design of many analog and digital devices, as well as directing the activities of other engineers and technical people working on the project. Among the systems successfully built and shipped under his direction were a high speed rocket test stand digital data system for Rocketdyne, McGregor, Texas, and two high-speed nuclear reactor temperature monitoring and safety circuit control systems, Hanford, Washington.

Previously, Mr. Larson was with Hallamore Electronics (Division of Lear Siegler, Inc.) where he was responsible for the circuit design of the deflection circuits for an Airborne Image Orthicon Camera System and various FM-FM telemetry circuits.

Mr. Larson received his BSEE degree from the University of California at Berkeley in Engineering Physics.

APPENDIX A.
SPECIFICATION FOR A ONE-GIGABIT DISK FILE

1. SCOPE

1.1 This specification covers the requirements for design, fabrication, documentation and performance requirements of a One-Gigabit File.

1.1.1 The equipment shall be capable of operating in an airborne environment as specified herein.

1.1.2 General - The One-Gigabit File shall functionally comprise a main store and an input/output section, together with power supplies necessary to operate it.

1.1.3 Memory Type - The main store shall include rotating magnetic disks and associated selectable, roving recording, and reproducing equipment.

2. APPLICABLE DOCUMENTS

2.1 The following documents of the issue shown form a part of this specification to the extent specified herein.

Specifications

Military

MIL-E-5400H - Electronic Equipment Aircraft, General Specification for

MIL-STD-826 - Electromagnetic Interference Test Requirements and Test Methods

MIL-I-6181 - Interference Control Requirements Aircraft Equipment

MIL-T-5422 - Testing, Environmental, Aircraft Electronic Equipment

MIL-D-1000 - Dated 1 March 1965 - Drawings, Engineering and Associated Lists

MIL-B-5087 - Bonding, Electrical for Aircraft

MIL-STD-704 - Electrical Power Aircraft Characteristics

MIL-I-45208A - Inspection System Requirements

RCA 1890613 - ADA Grounding Specification

MIL-STD-243 - Types and Definitions of Models for Communications and Electronics Equipment

2.2 The following document will be used as a design guide:

MIL-S-38130A- Safety Engineering of Systems and Associated Subsystems and Equipment, General Requirements for

3. REQUIREMENTS

3.1 Precedence of Specifications - In the event of conflicts between different specifications, this specification shall have precedence over all others.

3.2 Type - The File shall be an Exploratory Developmental Model as defined in MIL-STD-243, except that it shall have the required final form factor and employ approved parts or their interchangeable equivalents.

3.3 Non-Standard Parts - Non-standard parts shall meet the general material and environmental conditions as specified in MIL-E-5400H.

3.4 Standard Parts - Military standard parts shall be used wherever they are suitable and shall be identified by their applicable part number.

3.5 Material and Parts - Material shall be in accordance with requirements of MIL-E-5400H, except as otherwise specified herein.

3.5.1 Solid State Devices - Solid State Devices and circuits such as microelectronic circuits, tunnel diodes, transistors, magnetic cores, and thin films, shall be employed to the maximum extent possible commensurate with good engineering practice to reduce equipment size and power consumption. Effort shall be made to minimize the number of different types of semiconductor devices.

3.6 Protective Treatment - Materials used in the construction of the unit that are subject to deterioration when exposed to climate and environmental conditions likely to occur during service usage shall be protected as follows:

A. They shall be protected against such deterioration in a manner that will in no way prevent compliance with the performance requirements of this specification.

B. The use of any protective coating that will crack, chip, or scale with age or extremes of climate and environmental conditions, as set forth herein, shall be avoided.

3.7 Interchangeability

3.7.1 Interchangeability - All electronic parts and modules having the same manufacturer's part number shall be functionally and dimensionally interchangeable.

3.7.2 Selected and Matched Parts - The use of selected and matched parts shall be kept to a minimum. Autonetics shall identify on the appropriate drawings, all selected or matched parts, i.e. purchased assemblies, balanced diode modulators, precision resistor networks, matched gears, etc.

3.7.3 Standardized Assemblies - Standard assemblies shall be utilized or developed wherever practicable. An assembly shall be considered standardized if it can be used in multiple applications with no basic change.

3.8 Service Conditions

3.8.1 Environmental Conditions - The File shall be designed to meet the environmented conditions set forth in MIL-E-5400H, Class 1A, while being subjected to any probable combination of the following environmental conditions.

3.8.1.1 Storage Life - The equipment shall be capable of being stored for a period up to one year prior to operation.

3.8.2 Non-Operating - The equipment shall be designed to meet operative requirements after being subjected to these conditions.

3.8.2.1 Humidity - Relative humidity up to 95 percent may occur with conditions such that condensation takes place in the form of water, except that conditions causing actual condensation within the equipment during non-operation shall require a "dry out" operation before startup.

3.8.2.2 Altitude - Altitude may vary from sea level to 40,000 feet.

3.8.2.3 Temperature - The File shall be designed to meet a range of -55°C to 75°C.

3.8.2.4 Vibration - The File shall be designed to meet the full vibration requirements of MIL-E-5400H, Curve IA, except that the maximum input shall not exceed ±5 g's.

3.8.2.5 Shock - The equipment will be designed to withstand shock of a free fall of 4 inches to the horizontal with only one edge resting on horizontal.

3.8.2.6 Crash Safety - The design of the File shall provide for crash safety at the levels of 16 g forward, 4 g downward, and 1.5 g side to side and aft. Crash safety environmental test will consist of imposing the above g loads on a mock-up dummy.

3.8.3 Operating - The following conditions occurring separately or in combination may be encountered by the equipment while aircraft is in use. These conditions are applicable to components at their installation interfaces. The equipment shall be designed to meet operative requirements as applicable during and/or after being subjected to these conditions.

3.8.3.1 Altitude - Altitude conditions will increase from sea level to 40,000 feet (5.89 inches of mercury pressure).

3.8.3.2 Temperature - The File shall be designed to meet an operating range of -40°C to +55°C.

3.8.3.3 Vibration - The File shall be designed to meet the full vibration requirements of MIL-E-5400H, Curve I, except that the maximum input shall not exceed ±5 g's.

3.8.3.4 Radio Interference and Susceptibility - The File shall meet the interference requirements of MIL-I-6181 above 150 kHz and the test limits of MIL-STD-826 Class AM from 15 kHz to (and including) 150 kHz.

The File shall meet the susceptibility requirements of MIL-I-6181 and in addition shall meet the radiated susceptibility requirement of MIL-STD-826 from 15 kHz to (and including) 150 kHz using drive levels which produce a field intensity at the Test sample equal to that produced by MIL-I-6181 test set-up at 150 kHz.

3.8.3.5 Angular Rates and Accelerations - Equipment will meet performance specifications while subjected to the following angular rates and accelerations of the aircraft.

3.8.3.5.1 Pitch angular accelerations of 52 deg/sec^2 and angular rate of 30 deg/sec.

3.8.3.5.2 Roll - Angular accelerations of 100 deg/sec^2 and angular rate of 45 deg/sec.

3.8.3.5.3 Angular acceleration of 16 deg/sec^2 and angular rate of 20 deg/sec.

3.9 Performance Characteristics

3.9.1 General - This specification covers the minimum requirements for a nonvolatile file.

3.9.1.1 The File shall have the following characteristic - Turn-off of power shall not affect the quality of information previously recorded (except the record being written when turn-off occurs).

3.9.1.2 The File shall be capable of storing 180 megabits of information, with the data word an integral number of 6-bit bytes not counting word parity (200 megabits, with the data word an integral number of 8-bit bytes).

3.9.1.3 Data may be transferred in parallel to and from the central data processor (CDP) as a 36-bit word plus parity. Parity shall be odd. Six bit groups plus parity in parallel transfer is alternately available.

3.9.1.4 The average access to the first word of any record is approximately 38 milliseconds.

3.9.1.5 The maximum access time to the first word of any record shall not exceed 100 milliseconds.

3.9.1.6 Data storage within the File may be organized so that access to the first word of any data block shall be random. The minimum data block shall be 51 words in length. Sixty-four data blocks shall be at any one access arm location. However, a record may contain variable length, i.e., less than a full data block, or more than an integral number of data blocks.

3.9.1.7 The File shall be capable of storing the full core (approximately 33K words) of the CDP without interruption once the initial address has been reached. The CDP shall provide and the File shall store the next access arm address prior to reaching the initial address, and then successively the next access arm address on completion of transfer of 3264 words, nine times. (The File can be designed to automatically position the access arms without the ten additional instructional words for continuous transfer of 33K words, or the complete file, i.e., from the beginning address through the last address of the instruction.)

3.9.1.8 Data transfers between the CDP and the File shall occur up to 65K words per second.

3.9.1.9 A record shall be identified in the File by a start address and record word length.

3.9.1.10 Each successive word of any record shall be stored consecutively.

3.9.1.11 The File shall be capable of detecting faulty data transfers from the CDP and informing the CDP of such errors.

3.9.1.12 The error rate for the equipment described in this specification shall not exceed one error for every 10^{11} bits transferred in or out of the File.

3.9.2 Interface Characteristics

3.9.2.1 General - This specification describes the interconnecting signal functions.

3.9.2.1.1 The interconnecting signals between the CDP and the File are divided into three categories: command signals, input transfers, and output transfers.

3.9.2.1.2 Command Signals - There will be a minimum of nine interconnecting command signals.

3.9.2.1.2.1 Peripheral Device Available (PD/AVL) - This signal will be generated by the File and will be a logical one whenever the File is available to process a CDP service request.

3.9.2.1.2.2 Central Data Processing Service Request (CDP/SVR) - This signal is generated by the CDP and will be a logical one when the CDP requests access to the File. A CDP/SVR will cause the File to release the PD/AVL line (logical zero) and decode the instruction word delivered to the File input register.

3.9.2.1.2.3 Data Available (DATA/AVL) - When the File decodes the instruction word as a read operation and also decodes a comparison between the current processing address and the desired address, the File shall send a DATA/AVL signal (logical one) to the CDP. The File shall also transmit the first word of the desired text to the CDP input register with the DATA/AVL signal.

3.9.2.1.2.4 Data Acknowledge (DATA/AKN) - The CDP will generate a DATA/AKN signal (logical one) when it is expecting to receive information (read op.), has received a DATA/AVL, and has detected the presence of at least one bit (parity, if necessary) in the CDP input registers. Upon receiving a DATA/AKN signal the File will release its DATA/AVL signal (logical zero). The release of DATA/AVL will cause the CDP to release the DATA/AKN signal.

The DATA/AVL and DATA/AKN signal sequence will take place for every word of data transferred during a read operation.

3.9.2.1.2.5 End of Data (EOD) - The File shall send a signal EOD (logical one) to the CDP when it detects the last record address.

3.9.2.1.2.6 Data Request (DATA/REQ) - When the File decodes the instruction word as a write operation and also decodes a comparison between the current processing address and the desired address, the File shall send a DATA/REQ (logical one) to the CDP.

3.9.2.1.2.7 Data Transferred (DATA/XFR) - Upon receipt of a DATA/REQ signal, when in the write mode of operation, the CDP will transfer a 37-bit word (36 data plus parity) to the File input register as well as a DATA/XFR (logical one) command signal.

Upon receipt of the data and a DATA/XFR signal, the File will release the DATA/REQ signal.

3.9.2.1.2.8 Priority Interrupt (PIR) - The CDP can create a priority interrupt signal which will cause the File to terminate the present instruction in a safe manner and decode the next data transfer as an instruction word. A CDP/SVR will be generated after the PIR.

3.9.2.1.2.9 Mass Memory Error Indicator (MME) - The File must under certain conditions generate a signal which will be interpreted by the CDP as an error indication. When the File generates an MME it will deliver to the CDP input register upon receiving a CDP/SVR an error word according to the format of Figure A-1. This error word will be decoded by the CDP and the CDP will generate its DATA/AKN signal. The DATA/AKN will cause the File to release its MME.

The specific instances under which the File can generate an MME are:

01. Illegal instruction word
02. Illegal message length
03. Illegal address
04. Address no compare
05. Write/erase not safe
06. Head selection not safe
07. Drive inoperative
08. Drive busy
09. Invalid data (parity error)
10. Over temperature
11. Pressure cut-off

3.9.2.2 Input Register - The File will provide a 37-bit data input register. The input register will be used for receiving both data inputs and instruction words. See Figure A-1 for generalized data and instruction word format.

3.9.2.3 Output Register - The File will provide a separate and distinct (from input register) 37-bit data output register. This register will be used for transmitting data and error words to the CDP. See Figure A-1 for generalized format.

3.9.3 Instruction Word - The instruction word can be subdivided into three distinct sub-instruction words.

3.9.3.1 Operational Sub-Instructions - The instruction word will contain a subfield which defines the mode of operation. The following functions will be included within the operational codes.

A. Restart - Initialize the File when its status is unknown.

B. Transfer Error Conditions - Transfer of error word to the CDP.

C. Seek Index - Search for initial address within a selected band.

D. Write Address - A write address instruction for writing memory sub-division addressed.

E. Write Data Mode - Further defined as to what sub-division mode is requested.

F. Read Data Mode - Further defined as to what sub-division mode is requested.

G. Sub-Division Modes - Sector, track or band. Modes of reading or writing are to be incorporated.

3.9.3.2 Address Sub-Instruction - An address sub-instruction is required. It is intended that the address sub-instruction completely define the storage area within the File to be operated upon. It is further intended that protected areas of the File be defined by the sub-instruction. Protected areas are those File sub-areas limited to read only operations during normal operation. Modifying a protected area can only be accomplished by manually setting a manual switch to allow the processor to write in the protected area.

Actual bit allocation for the operation code and address sub-instruction will be specified prior to procurement.

3.9.3.3 Record Length Sub-Instruction - A 15-bit structure which defines the length of the record to be processed. The record length in conjunction with the address specified in paragraph 3.9.3.2 will define the starting and ending of all records processed.

3.9.4 Electrical Interface - All communications between the File and the CDP will be over co-axial cables with appropriate line drivers and receivers on the transmitting and receiving ends. The co-axial cable and connector will be specified prior to contract award. The specific design of the line drivers and receivers used by Autonetics shall be submitted to the contractor for approval.

3.9.5 Documents - In addition to any mechanical or logic schematics required, Autonetics shall supply ten copies of operational manuals and ten copies of program manuals.

3.10 Equipment Description

3.10.1 Size - The File shall be of such size as to be enclosable in a 24" × 24" × 27" rectangular parallelepiped. Total size does not include mounting supports or cables.

3.10.2 Weight - The design goal shall be 250 lbs. Total weight does not include mounting supports or cables.

3.10.3 Power - The File shall be designed to operate with power inputs of 115 VAC, 400 cps, 3 ϕ, not to exceed 500 watts, and 28 VDC not to exceed 1200 watts, per MIL-STD-704, Category B.

3.10.4 Reliability - The design goal for reliability shall be in excess of 3200 hours mean time between failure (MTBF).

3.11 Maintainability

3.11.1 Maintenance - Maintenance and replacement, where feasible, shall be on a modular basis. All circuitry shall be packaged in easily replaceable modules. All electronic sub-assemblies, power supplies, and blowers (if required) shall be readily accessible to the operator.

3.11.2 Mean Time to Repair - Design goal shall be 30 minutes for mean time to repair the electronics after the dust and drip-proof covers have been removed from the electronics compartment.

3.12 Design and Construction

3.12.1 General Design Features - For purposes of description the File may be considered in two separate packages. These packages shall be one structurally integral package in the complete unit.

3.12.2 Electromechanical Package - All dynamic elements in the File shall be enclosed in a "hermetically" sealed package to maintain a controlled atmosphere to assure proper functioning of the gas bearings in the system. This package includes the rotating magnetic disk stack and all associated moving and stationary recording and reporducing equipment, together with the necessary bearings and drive motors.

3.12.3 Electronic Module Package - All replaceable electronic modules shall be located in a dust- and drip-proof package outside the hermetically sealed region. This package shall include the various logic modules, servo amplifier units, I/O buffers, power supplies, and other electronics.

3.12.4 Accessibility - All electronic modules shall be readily accessible when the environment covers are removed.

3.12.5 Drawings - Drawings shall conform to MIL-D-1000, Category A and B, Form 3. Logic diagrams will be prepared in accordance with MIL-STD-806B.

3.12.6 Orientation - The File shall be designed to operate in any position.

3.12.7 Bonding - The File will meet the requirements of MIL-D-5087 (ASG) Bonding Specification.

3.12.8 Grounding - Grounding will be in accordance with ADA Grounding Specification RCA 1890613.

4. QUALITY ASSURANCE PROVISIONS

4.1 General - The quality assurance program shall be governed by MIL-I-45208A.

4.2 Inspection Requirements - The supplier is responsible for the performance of all inspection requirements as specified herein. Except as otherwise specified, the supplier may utilize his own or any other facilities and services in the performance of inspection. Inspection records of the examinations and test shall be kept complete and available as specified in the contract or order.

4.3 Environmental Tests - The supplier shall perform tests in accordance with MIL-T-5422 to determine if the equipment meets environmental requirements specified herein.

4.4 Acceptance Tests - Acceptance tests shall be conducted at the supplier's plant on the equipment to determine its acceptability. Supplier will conduct tests which are requisite to assure that the equipment meets performance requirements for capacity, access, I/O data rate, and I/O conformance as specified herein.

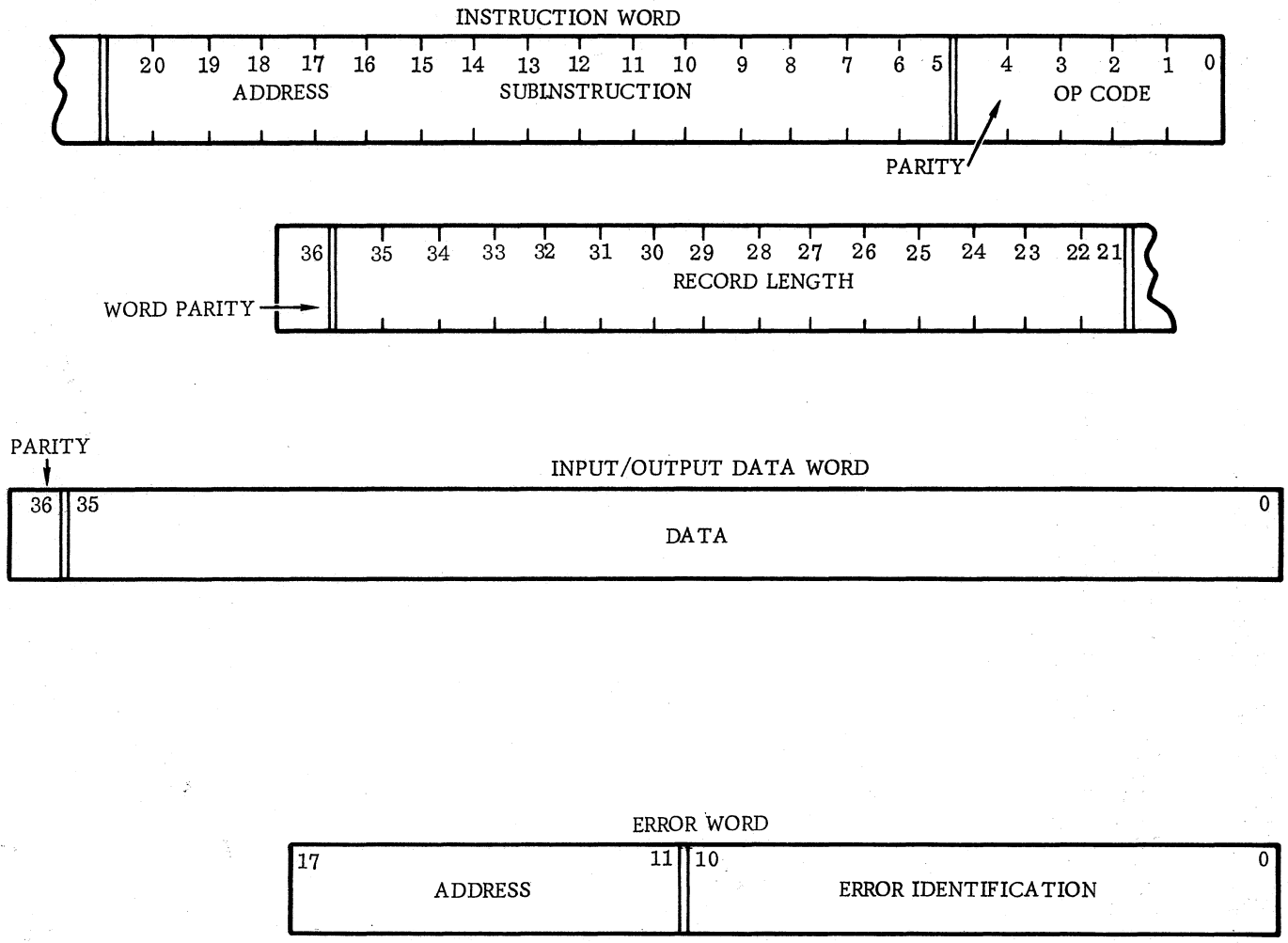

Figure A-1. Generalized Word Format

APPENDIX B. INTERFACE TIMING

1. END OF DATA (EOD)

This pulse shall occur not less than 500 nanoseconds nor more than two microseconds after the leading edge of the DATA/AVL or DATA/REQ pulse corresponding to the last character or word of the record is transferred to or from the data processor.

2. DATA OUTPUT SIGNALS (DO)

The file shall provide a set of signals for transferring data to the external data processor. The data will be transferred in groups of six bits in parallel (one character at a time) plus one bit to provide odd parity for the seven bits. The File will also be capable of data transfers effected in groups of 36 bits in parallel (one word at a time) plus one bit odd parity for the 37 bits.

3. TIMING (DO)

For each character or word transferred, the DO signals shall assume the proper values at least 200 nanoseconds before the leading edge and at least 200 nanoseconds after the trailing edge of the DATA/AVL pulse. The DO signals shall remain available to the external data processor for at least 75 percent of the character (or word) transfer time.

4. DATA INPUT SIGNALS (DI)

The external data processor will provide a set of signals for transferring data to the file. The number of bits transferred, the format, and the rates will be the same as the DO signals.

5. TIMING (DI)

For each character or word transferred, the DI signals will assume the proper values not more than 200 nanoseconds after the leading edge of the DATA/REQ pulse. The DI signals will remain available to the file for at least 75 percent of the character (or word) transfer time.